whereby the gate of the first transistor and the gate of the third transistor are coupled together and are both connected to a DC voltage.

REMARKS

The October 4, 2001 Office Action was based upon pending Claims 13-15 and 17. By this Amendment, Applicant amends Claim 13. Thus, after entry of this Amendment, Claims 13-15 and 17 are pending and presented for further consideration.

The specific changes to Claim 13 are shown on a separate set of pages attached hereto and entitled **VERSION WITH MARKINGS TO SHOW CHANGES MADE**, which follows the signature page of this Amendment. On this set of pages, the insertions are underlined while the ~~deletions are struck through~~.

Claim Rejections

The Examiner rejected Claims 13-15 and 17 under 35 U.S.C. § 102(e) as being anticipated by Buhler (U.S. Patent No. 5,742,047). As to Claim 13, the Examiner asserted that Buhler discloses a pixel having a photosensitive element (D1) and first, second and third transistors (M1, M4, M2) that are connected as defined in Claim 13. Further, the Examiner asserted that the gate of the first transistor and the gate of the third transistor are coupled together to a DC voltage (Φ_{DR} and V_{TI}). Applicant respectfully disagrees with the Examiner's analysis of Buhler.

In particular, Applicant submits that Buhler does not disclose or suggest the limitation "*whereby the gate of the first transistor and the gate of the third transistor are coupled together to a DC voltage.*" It appears that the Examiner maintains that the gates of the transistors M2 and M1 are coupled together to a DC voltage. However, this is incorrect because the gate of the transistor M1 is coupled to the clock signal Φ_{DR} whereas the gate of the transistor M2 is coupled to the DC transfer gate voltage V_{TI} (column 3, lines 10-19). Buhler's Figure 1 unambiguously shows that the gates of the transistors M1 and M2 are not connected together.

With Buhler failing to disclose that the gate of the first transistor and the gate of the third transistor are coupled together to a DC voltage, Applicant respectfully submits that Buhler does

not disclose each and every element of Claim 13. However, in order to clarify any existing misunderstanding of the claim language, Applicant has amended Claim 13 to further define that the gate of the first transistor and the gate of the third transistor are coupled together and are both connected to a DC voltage. For the reasons set forth above, Applicant submits that Claim 13 as amended is not anticipated by Buhler.

Furthermore, Buhler provides no suggestion for a pixel as defined in Claim 13 as amended. The fact that in Buhler the gate of the transistor M1 is coupled to the clock signal Φ_{DR} whereas the gate of the transistor M2 is coupled to the DC transfer gate voltage V_{TI} indicates that Buhler's pixel is based on a structure and operation that are different from the pixel of Claim 13. In fact, Buhler's different structure prohibits one of ordinary skill in the art to connect the gates. A clock pulse (Φ_{DR}) and a gate transfer voltage (V_{TI}) are two different things. The voltage applied to the gate of the transistor M2 is designed to ensure that pass transistor M2 is in its saturation region (column 4, lines 21-31). The advantage is that the current through this transistor M2 is then constant. This may occur at a gate voltage of 0 volts. Hence, Applicant submits that there is no relationship between the clock pulse (Φ_{DR}) and the gate transfer voltage (V_{TI}).

In view of the above remarks, amended claim 13 is novel and non-obvious over Buhler. Claims 14-15 and 17, which depend on claim 13, are also patentable. Accordingly, all claims are believed to be in the condition for allowance, and allowance is earnestly solicited.

CONCLUSION

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. In light of the above remarks, reconsideration and withdrawal of the outstanding rejections is specifically requested.

If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the Examiner is respectfully requested to initiate the same with the undersigned.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: Jan. 28, 2002

By: _____

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

The claims have been amended as follows:

13. (Twice Amended) A pixel for imaging applications fabricated in a MOS technology, said pixel comprising:

a photosensitive element and a first transistor having a gate and a first and second electrode and being in series with said photosensitive element, said first transistor and said photosensitive element thereby forming a first connection;

a second transistor having a gate, said second transistor being coupled to said first connection, thereby forming a second connection, and said second transistor being part of an amplifying circuit; and

a third transistor having a gate and having two electrodes, said third transistor being connected in said second connection between said first connection and said second transistor;

whereby the gate of the first transistor and the gate of the third transistor are coupled together and are both connected to a DC voltage.